LOW CAPACITANCE ESD-PROTECTION STRUCTURE UNDER A BOND PAD

ABSTRACT OF THE DISCLOSURE

An ESD-protection structure is located substantially under an integrated circuit bond pad. This ESD-protection structure is formed as a low capacitance structure by inserting a forward diode between the bond pad and the ESD clamp circuit. Placing the ESD-protection structure under the bond pad eliminates parasitic substrate capacitance and utilizes a parasitic PNP transistor formed from the inserted forward biased diode. The ESD-protection structure comprises adjacent alternating P+ and N+ diffusions located substantially under a bond pad to be ESD protected. The P+ diffusions are connected to the bond pad metal with metal vias through an insulating layer located between the bond pad and the P+ and N+ diffusions. The N+ diffusions are adjacent to the P+ diffusions. An N+ diffusion surrounds the N+ and P+ diffusions, and ties together the N+ diffusions so as to form a continuous N+ diffusion completely around each of the P+ diffusions. An N- well is located substantially under the N+ and P+ diffusions. The surrounding N+ diffusion partially overlaps the edge of the N- well below it. An outer portion of the N+ diffusion, the portion overlapping the N- well, is within a P- well. The P- well may be the substrate of the integrated circuit. Another N+ diffusion encircles the N+ diffusion surrounding the P+ diffusions. The another N+ diffusion is in the P- well and a field oxide may be located between the N+ diffusion and the another N+ diffusion. An NPN field transistor is formed with the N+ diffusion being the transistor collector, the P- well being the transistor base and the another N+ diffusion being the emitter. The another N+ diffusion (emitter) may be connected to ground by a conductive connection, *e.g.*, metal or low resistance semiconductor material.